Yichen Yang

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Summary

I am a Ph.D. student at the University of Michigan, advised by Ronald Dreslinski. My main research interest and experience lies in general computer architecture, hardware accelerators and reconfigurable architecture.

Education

University of Michigan, Ann Arbor, MI, U.S.A. 2019 – 2024 (Expected)

Ph.D. in Computer Science and Engineering

- Advisor: Ronald Dreslinski

University of Michigan, Ann Arbor, MI, U.S.A. 2019 – 2021 (Expected)

M.S.E in Computer Science and Engineering, GPA: 4.0/4.0

- Relevant coursework: EECS573 Micro-Architecture, EECS598 Applied Parallel GPU Programming (A+), EECS545 Machine Learning (A), EECS583 Advanced Compilers

University of Michigan, Ann Arbor, MI, U.S.A. 2017 – 2019

B.S.E in Computer Engineering, GPA: 3.91/4.0

- Relevant coursework: EECS470 Computer Architecture (A+), EECS482 Operating System, EECS570 Parallel Computer Architecture (A+), EECS442 Computer Vision (A), EECS498 Deep Learning (A), EECS484 Database Management System

Shanghai Jiao Tong University, Shanghai, China 2015 – 2019

B.S.E in Electrical and Computer Engineering, major GPA: 3.70/4.0

Publication

- **Prodigy: Improving the Memory Latency of Data-indirect Irregular Workloads using Hardware/Software Co-design**
  IEEE International Symposium on High-Performance Computer Architecture (HPCA) 2021
  - Nishil Talati, Kyle May, Armand Behroozi, **Yichen Yang**, Kuba Kaszyk, Christos Vasiladiotis, Tarunesh Verma, Lu Li, Brandon Nguyen, Jiawen Sun, John Magnus Morton, Agreen Ahmadi, Todd Austin, Michael O'Boyle, Scott Mahlke, Trevor Mudge, Ronald Drelinski.
- **CoPTA: Contiguous Pattern Speculating TLB Architecture**
  International Conference on Embedded Computer Systems: Architectures, Modeling and Simulation (SAMOS) 2020
  - **Yichen Yang**, Haojie Ye, Yuhan Chen, Xueyang Liu, Nishil Talati, Xin He, Trevor Mudge, Ronald Dreslinski.
- **Parallelism Analysis of Prominent Desktop Applications: An 18-Year Perspective.**
  IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) 2019
  - Siying Feng, Subhankar Pal, **Yichen Yang**, Ronald Dreslinski.

Research Experience

CADRE Lab Dec. 2017 – Present

Graduate Student Research Assistant, Sep. 2019 - Present
Undergraduate Student Research Assistant, Dec. 2017 - Apr. 2019

- Advised by Prof. Ronald Dreslinski

Industry Experience

Apple Inc. May. 2021 – Aug. 2021

Hardware Technology Research Internship with CPU Design & Verification Team

Notable Projects

Hardware-Software Co-Designed Cache Bypass Mechanism on X86 Machine Oct. 2020 – Dec. 2020

EECS 583 - Advanced Compilers Research Project, Group Project, Leader

- In this project, we build an end-to-end HW-SW co-designed tool chain including compiler and hardware simulator modification to show that cache bypass brings performance gains to X86 machine under some circumstances.

Understanding Indoor 3D Geometry from AmbientSounds Jan. 2020 – Apr. 2020

EECS 545 - Machine Learning Research Project, Group Project

- In this project, we demonstrate ambient sounds are able to perform these tasks under certain constraints, and analyze representative failure cases. Additionally, we show we can train a comparable model using visual depth estimation as pseudo-labels.

CNN Kernel Optimization with CUDA Mar. 2020 – Apr. 2020

EECS 598 - Applied Parallel GPU Programming, Group Project, Leader

- In this project, we optimized the CNN (Convolutional Neural Network) kernel with CUDA. By utilizing constant memory and exploring parallelism opportunities in the code, we achieved 48X speed up.

Transmuter: Efficient General-Purpose Acceleration via Reconfiguration and Spatial Dataflow Jan. 2019 – Apr. 2019

EECS570 - Parallel Computer Architecture Research Project, Group Project

- Transmuter is a general-purpose accelerator design composed of light-weight cores and reconfigurable interconnects and memories. Through simple hardware reconfiguration mechanisms, Transmuter achieves state-of-theart efficiency on diverse kernels with disparate compute and data movement patterns.

Formal Verification of the MESI Cache Coherence Protocol Mar. 2019

EECS570 - Parallel Computer Architecture Course Project

- This is a individual project to verify the directory-based MESI cache coherence protocol using Murphi.

Text & Vision-Fused Framework for Academic Paper Review Jan. 2019 – Apr. 2019

EECS498/598 Deep Learning Research Project, Group Project, Leader

- We implemented a Text & Vision-Fused deep learning model, which can act as a pre-selector for academic paper review.

Out-of-Order Alpha 64 Processor Implementation Oct. 2018 – Dec. 2018

EECS470 - Computer Architecture Final Project, Group Project, Leader

- Design and implement a 2-way superscalar, R10K style out-of-order processor with System Verilog, including separate instruction and data caches, early tag broadcast, Tournament branch predictor with branch target buffer, return address stack, instruction prefetching, and a load-store queue with data forwarding.

Stacked Global History Register Branch Predictor Dec. 2017 – Aug. 2018

Undergraduate Research Assistant, Advised by Prof. Ronald G. Dreslinski

- Proposed and implemented a stack structure to the global history register (GHR) in an L-TAGE and Tournament branch predictor to achieve a per-function history register. Each function has its own branch history register, based on which to predict the next branch direction.

Single-view Surface Normal Prediction Mar. 2018 – Apr. 2018

EECS442 - Computer Vision Final Project, Group Project, Advised by Prof. Jia Deng

- Develop a machine learning model using stacked hourglass ConvNet to predict the surface normal of a object from a single view image. Our result has 0.356 MAE (mean angle error) accuracy and breaks the record from last year.

EECS482 Operating System Course Projects Feb. 2018 – Apr. 2018

EECS482 - Operating System Course Project, Group Project, Leader

- This includes 4 separate projects that implement parts of a operating system with C++. They are a multi-threaded disk scheduler, a thread management library, a virtual memory manager and a networked file system.

Skills

- Programming Language/Tools: C++, C, Python, CUDA, Java, Shell, Verilog, LLVM, gem5, Sniper-Sim
- Operating Systems: Linux, Windows

Teaching

- EECS470 Computer Architecture Instruction Assistant Winter 2019
- VG100 Intro. to Engineering Teaching Assistant Summer 2017

Honors, Awards and Scholarship

- James B. Angell Scholar Mar. 2020
- University of Michigan Honors Dec. 2017, May. 2019
- University of Michigan, College of Engineering Dean's List Dec. 2017, Dec. 2018, May. 2019
- SJTU Outstanding Undergraduate Student Scholarship Nov. 2016, Nov. 2017
- UM-SJTU Joint Institute Dean's List Oct. 2016